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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,577	08/18/2003	Gregory J. Faanes	1376.711US1	3947

21186 7590 11/02/2006

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,577	FAANES ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,12-22 and 24-32* is/are pending in the application.

4a) Of the above claim(s) *1-6,16-21 and 26-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,8,12-15,22,24,25 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 8/21/2006. Claims 1-6, 16-21, and 26-28, have been withdrawn in response to the confirmed election of Group II. Claims 9-11 and 23 have been canceled and claims 29-32 are new leaving claims 7, 8, 12-15, 22, 24, 25, and 29-32 are currently pending. Applicants' arguments and amendments have been carefully considered, but they are not persuasive and do not place the claims in condition for allowance. Accordingly, this action has been made FINAL.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Response to Arguments/Amendments

Applicant argues on page 12, second paragraph, of the current response:

> Hughes does not teach or suggest processing a memory request by comparing an address to addresses within local cache while, *at the same time*, comparing the address to partial addresses stored in an FOQ ...

Applicant's amended limitations of independent claim 7, 22, and 29, while claiming "processing a memory request in both a local cache and a Forced Order Queue," does not specifically claim that the memory request is processed in the FOQ and the local cache *at the same time*. Applicant also argues on page 12, paragraph 4:

> ... some of the memory requests are *not sent* to the second memory request container

> *after checking a cache* ... read requests that hit in the Dcache and have no potential matches in the FOQ are serviced immediately and are *not sent to the FOQ*.

Neither of the arguments presented by the Applicant are founded by claim limitations in the amended claims.

The Examiner has cited further sections of the Hughes reference to teach the amended limitations presented in the current set of amended claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7,8,12,13,22, and 29-32, are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes (U.S. Patent No. 6,393,536).

As per claim 7, Hughes teaches:

(1) **obtaining a memory request** [14/20-24];

(2) **storing the memory request in an Initial Request Queue (IRQ)** (LS1 buffer 60 - [14/20-24];

(3) **processing the memory request from the IRQ by a cache controller** [15/1-5] **wherein the processing includes:**

(4) **identifying a type of the memory request** [16/17-18];

(5) **processing the memory request in both a local cache and an Forced Order Queue (FOQ)** (LS2 buffer 62 - processing the request entails determining a miss or hit in the local

cache 28 [12/35-55], and processing the request in the FOQ 62 is taught among of sections at [17/1-40]. Further, **processing includes determining if a portion of the address** (i.e. the "tag" - [17/67 - 18/2]) **associated with the memory request matches one or more partial addresses** (tag bits) **in the FOQ** (one such instance is taught in [18/18-24], where the incoming load request's address is compared to the other older store addresses in the FOQ to forward matched data), **and if the memory request misses in the cache** [17/6-8] **and the address does not match one or more partial addresses in the FOQ** (i.e. for example a load that does not have a matching address for an older store is stored in the FOQ 62 - [18/9-30]), **adding the memory request to the FOQ** ([18/11-13] and [17/5-8]) **and allocating a cache line in the local cache corresponding to the local cache miss** [12/56-61].

As per claim 8, Hughes teaches **the obtaining of the memory request includes obtaining a memory load or a memory store request** in [16/17-18].

As per claim 12, Hughes teaches **processing the memory request includes processing the memory request using the FOQ when the memory request matches a corresponding request in the FOQ** [18/11-30]. Here, Hughes teaches that younger load requests can be fulfilled by older store requests when the address of the younger load and the older store coincide and the data for the older store is available. As a result of these conditions, data from the older store is forwarded to the younger load.

As per claim 13, Hughes teaches **adding the memory request to the FOQ when the memory request is not initially processed by the local cache** (i.e. cache miss). In order to match a corresponding request in the FOQ so that the memory request can be processed by the FOQ, a --match-- in the FOQ requires a pending FOQ entry to have (1) a coincident address with

the incoming memory request and (2) available store data. Therefore, a memory request which is not initially processed by the local cache (a miss in data cache 28) and sent to the LS2 buffer (FOQ 62) and further does not --match-- a pending LS2 entry, is added to the FOQ as taught in the aforementioned passage, [18/24-30].

As per claim 22, Hughes teaches a **scalar processor** (figure 1) which **comprises:**

(1) **a cache** (data cache 28);

(2) **an IRQ** 60 (figure 3);

(3) **a cache controller** (combination of logic circuits 64 and 66);

(4) **wherein the IRQ buffers a scalar load/store command having a scalar load/store instruction and one or more addresses** (shown in figure 3 as receiving the load/store instruction tags 48 and address from elements 70) **and sends the scalar load/store command to the cache controller** (via bi-directional bus shown between the IRQ 60 and controller portion 64 - figure 4) **and the cache** 28 (via port 1 through MUX 74 - figure 3);

(5) **wherein the cache services the scalar load/store command received from the IRQ when the scalar load/store command hits in the cache** [12/44-47];

(6) **wherein the cache controller includes a FOQ** (LS2 buffer 62), **wherein the scalar load/store command is added to the FOQ when the scalar load/store command misses in the cache** 28 [17/6-8]; and

(7) **wherein one or more lines in the cache** 28 **are allocated for cache line replacement when the scalar load/store command is added to the FOQ** [12/56-61] **and the address for the cache line does not match a partial address in the FOQ** ([17/66 - 18/2] and

for example a load that does not have a matching address for an older store is stored in the FOQ 62 - [18/9-30]).

As per claim 29, the rejection follows the rejection for claim 22, with one modified interpretation - the Examiner is considering the cache controllers to be (1) a combination of the LS1 60 and the LS1 control logic 64 and (2) the other cache controller to be the combination of the LS2 62 and the LS2 control logic 66. In addition, Hughes teaches **a plurality of cache controllers** (controllers 64 and 66 - figure 3), and **the IRQ** 60 **sends the scalar load/store command to the cache (one of the cache and the cache controllers)** - as shown in figure 3 via port 1 with use of the MUX 74. The cache controller 66 includes a FOQ 62 as shown in figure 3.

As per claim 30, Hughes teaches **wherein the cache controller with the FOQ includes a FOQ index array**, which the Examiner is considering to be the memory element that contains the LS2 buffer 62 entries as shown in figure 3 and in detail in figure 5. Alternatively, because there is not any functional structure associated with the limitation of a index array, the Examiner could also interpret an "index array" to be the dependency link file 104 associated with the LS2 controller logic 66 as shown in figure 4. The dependency link files shows and index array containing lists of load instructions and a corresponding store data.

As per claims 31 and 32, the Applicant defines the phase "logically divided into a first and second queue" as "logically two separate queues unified into a single structure" - page 17, line 21. Hughes teaches a "unified structure" for the FOQ 62 since the FOQ comprises both loads [17/5-7] and stores [18/19-24]. The "first queue" of all of the loads stored within the FOQ 62 manages requests to memory as some of the loads miss the cache 28 [17/6-8] and therefore need to access the next level of memory to access the requested data (as well known in the art of

caching). The "second queue" of all of the store requests in the FOQ 62 manages the data to be stored in the cache [18/20-24]. Hughes goes on to teach that the FOQ 62 may be a FIFO [18/61 - 19/5], as the Applicant defines a "queue" - page 17, lines 21-24, of the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes (U.S. Patent No. 6,393,536) in view of Yamahata (U.S. Patent No. 5,247,639).

As per claim 14, Hughes teaches a multiprocessing system in figure 13 and [32/47-56] with processors 10 and 10a independently connected to the bus bridge 202 for connection to main memory 204. Hughes does not specifically teach **processing the memory request in the FOQ when local when local cache processing is bypassed**. Yamahata teaches a cache bypass bit for use when multiple processors are to obtain synchronization by using semaphore data in [2/4-38]. Specifically Yamahata teaches in [2/15-19] that an instruction decoder sends a bypass request to a bus control unit to bypass a local cache. Hughes shows a bus interface unit 37 connected to the load/store unit 26 in figure 2. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the multiprocessing system of Hughes with the cache bypassing during multiprocessor

synchronization teaching of Yamahata in order to have been able to maintain a level of cache coherency between the processors 10 and 10a of modified Hughes when both processors would be attempting to update main memory 204. The utilization of semaphore data instructions are well known in the art to be utilized in multiprocessing systems for contention of a shared resource (in the case of Hughes, it would be main memory 204).

As per claim 15, the rejection follows the rejection of claim 14, supra. Local cache processing is bypassed when the memory request includes a synchronization request (i.e. via a cache bypass bit 801 - [7/23-35]). The memory request can be seen to be a **synchronization request** since the bypass bit would be set in a memory request when attempting to access semaphore data to attain synchronization between the multiple processor 10 and 10a of modified Hughes 10 and 10a [2/35-38 Yamahata.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes (U.S. Patent No. 6,393,536).

As per claim 24, Hughes teaches that in one specific implementation of the present embodiment of the invention, the data cache 28 comprises an **address generator** (address translation circuitry) **to generate one or more physical addresses from the one or more addresses of the scalar load/store command** [17/20/23]; however, Hughes does not specifically teach the address generator being a part of load/store unit 26. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the load/store unit 26 of Hughes by implementing the address translation circuitry as part of the load/store unit 26 instead of the data cache, since it has been held that rearranging parts of an

invention involves only routine skill in the art. Refer to MPEP § 2144.04(vi). Such a modification would have increased the speed in which translated addresses are written into the LS2 buffer by not having to send the translated physical address across the address bus 80 [17/34-37].

As per claim 25, Hughes teaches **wherein the address generator** (address translation circuitry) **generates the one or more physical addresses using a translation look-aside buffer (TLB)** [17/27-31].

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The Examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

PIERRE BATAILLE
PRIMARY EXAMINER
10/30/06